Int. J. on Recent Trends in Engineering and Technology, Vol. 9, No. 1, July 2013

# Low Power VLSI Design of Modified Booth Multiplier

Shweta S. Khobragade[1] and Swapnili P. Karmore[2]
[1] G.H Raisoni College of Engineering, Nagpur, India
khobragadeshwe@gmail.com
[2] G.H Raisoni College of Engineering, Nagpur, India
swapnali.karmore@raisoni.net

***Abstract*— Low power VLSI circuits became very vital criteria for designing the energy efficient electronic designs for prime performance and compact devices. Multipliers play a very important role for planning energy economical processors that decides the potency of the processor. To scale back the facility consumption of multiplier factor booth coding methodology is being employed to rearrange the input bits. The operation of the booth decoder is to rearrange the given booth equivalent. Booth decoder can increase the range of zeros in variety. Hence the switching activity are going to be reduced that further reduces the power consumption of the design. The input bit constant determines the switching activity part that's once the input constant is zero corresponding rows or column of the adder ought to be deactivated. When multiplicand contains a lot of number of zeros the higher power reduction will takes place. therefore in booth multiplier factor high power reductions are going to be achieved.**

***Index Terms*— column bypass multiplier(CBM) , reverse body bias(RBB) , Digital signal processing(DSP).**

## I. Introduction

Advances in electronics technology have led to more effective encryption of data ,additional reliable transmission of information, and additional embedded intelligence in systems particularly ,to fulfill the increasing market demand for portable applications, these electronics devices consume very low power consequently, numerous digital signal process chips are currently designed with low power dissipation .in such systems [1],[2] a multiplier factor may be a basic arithmetic unit. The computation of a multiplier factor manipulates 2 input data to generate several partial products for resultant addition operations ,that within the cmos circuit design ,need several switching activities. thus, switching activities among the functional units of a multiplier as given within the following where the switching activity parameter is the loading capacitance, and operational voltage and the operational frequency may also be viewed because the effective switching capacitance of the transistors nodes on charging and discharging .therefore minimizing switching activities will effectively scale back power dissipation while not impacting the circuits performance.

Multiplications are basic arithmetic operations used virtually in all applications involving digital signal processing. One amongst the key ideas in low power design is eliminating spurious signal transitions [3]. Techniques such as clock gating, signal bypassing and delay standardization for simultaneous transition are projected to cut back the circuit activities. By increasing the amount of zeros conjointly we tend to cut back the switching activity .If the switching activity is reduced then power consumed by this circuit are going to be reduced. The number of gates per chip area keeps on increasing, whereas the gate switching energy does not decrease at constant rate. therefore the power dissipation rises and removal of heat becomes difficult and expensive.

The dynamic power of CMOS circuits is turning into a significant concern within the design of devices. There are completely different multiplier factor structures which may be classified as Serial Multipliers, Parallel multipliers, Array multipliers, Tree multipliers and then on[5]. Multipliers area unit categorized in relative to their design, applications, and also the means of producing partial product and summing up of partial product to produce the ultimate result. The computation can be disabled by either freezing its inputs or gating the logic evaluation. The former approach requires either input gating or multiplexing circuits while the latter approach needs extra gating logic along the evaluation path. The output signal bypassing must be realized by a multiplexer.

## II. Literature Review

### *A. Array multiplier*

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. With its good structure, this multiplier is based on the standard add and shift operations. Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits[5].

Conclusion: Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased[8]; due to this array multiplier is less economical .Thus, it is a fast multiplier but hardware complexity is high .


DOI: 01.IJRTET.9.1.31

*B) column bypass multiplier*

low power Column bypass multiplier design methodology that inserts more number of zeros in the multiplicand thereby reducing the number of switching activities as well as power consumption. The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated [1]. If multiplicand contains more zeros, higher power reduction can be achieved. To reduce the switching activity is to shut down the idle part of the circuit, which is not in operating condition[4].

Conclusion: The limitation of this technique is that number of column switched depends on the number of ones in the multiplicand .for example if the multiplicand is of 16 bit length as 1111111111111111 then all the full adders in the columns will get switched and consume more power[9] .less switching activity of components can be achieved if multiplicand contains more number of zeroes than ones.

## II. Multiplier

Multipliers have massive space, long latency and consume considerable power. Reduction of power consumption makes a device reliable. Therefore low power multipliers with high clock frequencies play a crucial role in today's digital signal processing. Digital signal processing (DSP) is that the technology at the center of succeeding generation of private mobile communication multiplication systems. Most DSP systems incorporate a multiplication unit to implement algorithms like convolution and filtering. Multiplications square measure basic arithmetic operations used just about all told applications involving digital signal processing. Multiplications will be thought about as a series of recurrent additions. Style of transportable battery operated transmission device needs energy economical multiplication circuits.

Multipliers are classified by the format in which words are accessed namely:

1. Serial multiplier.
2. Parallel multiplier.
3. Serial-parallel multiplier.

*1) Serial Multiplier*

Serial multipliers are popular for their low area and power .It uses a successive addition algorithm .It has a simple structure because both the operands are entered in a serial form Therefore the physical circuit requires minimum amount of area and less hardware reducing the data input pads to two[11].

*2) Parallel Multiplier*

Most of the digital systems incorporate a parallel multiplication unit to carry-out high-speed operation due to the operands is entered in parallel which consumes less time[10].

*3) Serial-Parallel Multiplier*

The serial parallel multiplier serves as a good tradeoff between time consuming serial multiplier and areas consuming parallel multiplier .These multipliers are used when there is a demand for both high speed and small area .In a device using serial-parallel multiplier, one operand is entered serially and the other is stored in parallel with a fixed[16].

## III. Design Of Multipliers

*A. Array Multiplier*

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. With its good structure, this multiplier is based on the standard add and shift operations. Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder the number of partial products depends upon the number of multiplier bits.

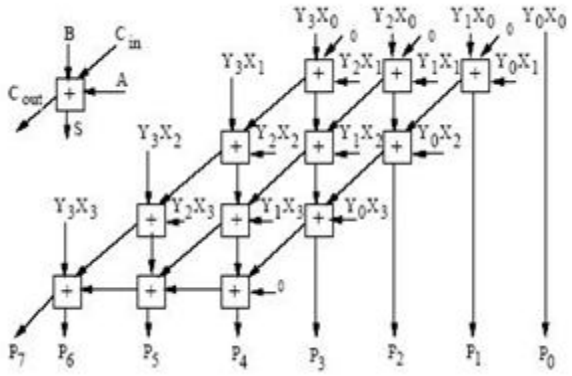


Figure 1 4x4 Array Multiplier

*B. Column Bypass Multiplier*

Instead of bypassing rows of full adders, we propose a multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages of this approach. First, it eliminates the extra correcting circuit as shown in Fig. 2.

## IV. Power Consumption In Cmos Circuits

Power is the most important parameter in digital circuits to Fabricate chips and portable devices. CMOS technology is used in digital circuits due to its less power consumption. Power consumption in CMOS circuits can be divided into Dynamic and static power consumption shown in eq (1)

$$P_s = \alpha F_{CLK} V_{DD2} C_L + I_{SC} V_{DD} + I_{LEAKAGE} V_{DD} \quad (1)$$

Where $\alpha$ is the switching activity, fclk is the clock frequency, CL is the output capacitance, VDD is the supply voltage, ISC is the short circuit current, and Ileakage is the leakage current. In micrometer technology dynamic power is the dominant Parameter while in the submicron technology, leakage current is the most dominant parameter in total power.





DOI: 01.IJRTET.9.1.31

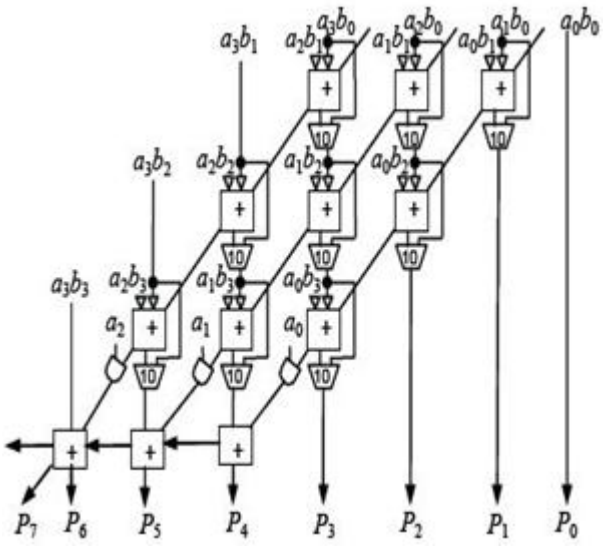


Figure.2 column bypass multiplier

The concentration of this paper is on leakage current reduction. In this paper we are going to reduce the leakage current using reverse body bias:

*A.Reverse Body Bias*

Reverse body bias technique is used to reduce leakage current during active operation, burn-in, as well as in standby mode. During active operation, RBB is applied to the idle portion of the chip to reduce overall chip leakage power without impacting the performance[14]. The subthreshold leakage is reduced when the body of the transistor is biased to a negative voltage with respect to the source of the transistor. The reduction in the leakage current is proportional to the extent of the applied reverse body bias. Since the chip operational frequency is very low during burn-in, RBB can be applied to the whole chip simultaneously[15].

## V. Proposed Design

*A. Modified booth multiplier*

Booth encoding is a method of reducing the number of partial products required to produce the multiplication result. To achieve high-speed multiplication, algorithms using parallel counters like modified Booth algorithm has been proposed and used. This type of fast multiplier operates much faster than an array multiplier for longer operands because it's time to compute is proportional to the logarithm of the word length of operands. By recoding the numbers that are to be multiplied, Modified Booth multiplier allows for smaller, faster multiplication circuits. The number of partial products is reduced to half, by using the technique of Booth recoding[6]. Reduction in the number of partial products depends upon how many bits are recoded and on the grouping of bits.

*B. Booth decoding Unit*

In this unit given multiplier is converted into an equivalent booth values. It contain more number of zeros. It uses the converting table as,

TableI:booth recoding table

| Block | Re - coded digit | Operation |
|---|---|---|
| 000 | 0 | 0 |
| 001 | +1 | +1 |
| 010 | +1 | +1 |
| 011 | +2 | +2 |
| 100 | -2 | -2 |
| 101 | -1 | -1 |
| 110 | -1 | -1 |
| 111 | 0 | 0 |

*C. Partial product generating Unit*

In this section, because the values of partial product bits are heavily dependent on the outputs of Booth encoders, we first explore the relation between the outputs of Booth encoders and the carry value propagated . Next, an effective and simple error compensation function, which takes the outputs of Booth encoders as inputs and then generates the approximate carry value, is derived to reduce the truncation error and make the error distribution as symmetric and centralized as possible.

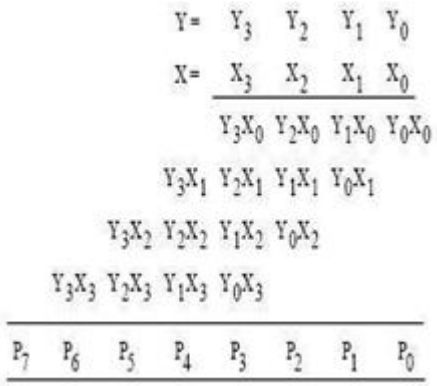


Figure 3: Partial product matrix for 4x4 modified Booth multiplication

## VI. Results And Discussions

*A. Array Multiplier*

Fig. 4. shows the design of array multiplier using S-Edit in Tanner tool. Initially all the basic gates (NAND Gate, NOR Gate, NOT Gate) are drawn using P and N MOSFET. Then by these gates normal adder circuit, Full adder circuit are drawn. Then by using these adders 4*4 Array multiplier is designed. The multipliers are X0-X3 and the multiplicand is Y0-Y3. The outputs are evaluated. As it is 4*4 Multiplier it's output is 8 bit. These outputs are seen in P0-P7.

Fig.5 shows the simulation result for the array multiplier design. In this 4 bit input is taken. The multiplier and multiplicand are 0101*0011. The output is read out in p0 to p3. Then the power consumption is evaluated using the power results.




DOI: 01.IJRTET.9.1.31

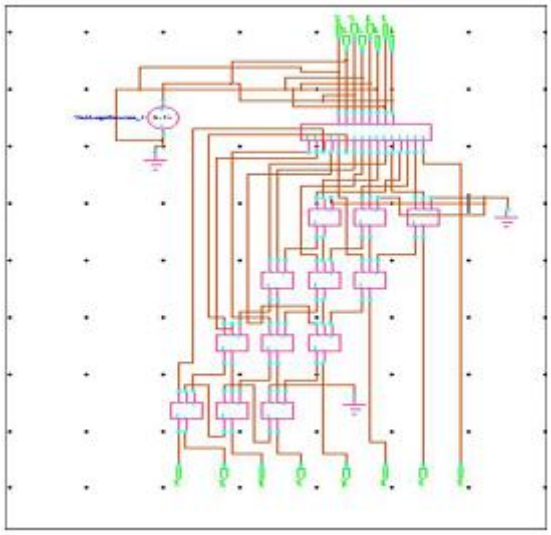

Figure 5: array multiplier

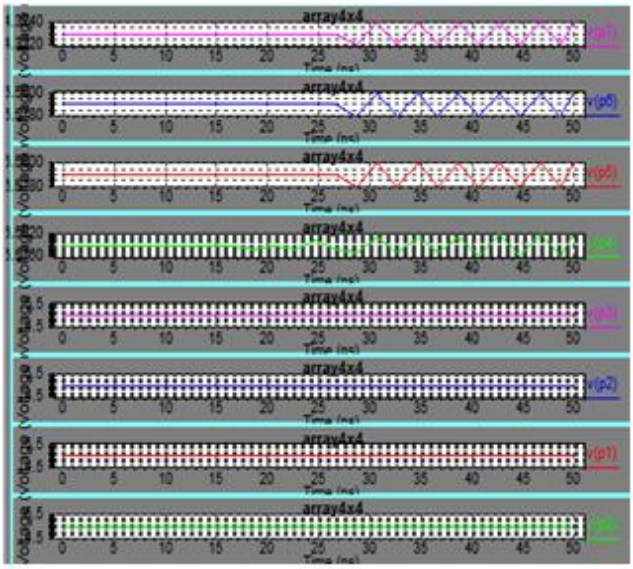

Figure.6. Simulation Result for the Array Multiplier Design

Power Results for array multiplier:
Average power consumed = 7.3936e-05watts

### *B. Column bypass multiplier*

Figure. 6 shows the design of Column Bypass multiplier using Conventional full adder is created using S-Edit in Tanner. Initially, XOR, INV (inverter) and MUX (multiplexer) are created using CMOS logic and by instantiating respective blocks circuit is drawn. Then by using these logics the design of the Column bypass multiplier is drawn. In this all controlling of conventional full adder is done by the input value a0-a3.Depending on the input of 'a' the whole full adder will be in on state or in off state. So the power consumption by the circuit is low when compared to the other circuits.

Fig. 7 shows the simulation result for the column bypass multiplier design. In this 4 bit input is taken. The multiplierm and multiplicand are 1111*1101. The output is read out in p0 to p7. Then the power consumption is evaluated using the power results.

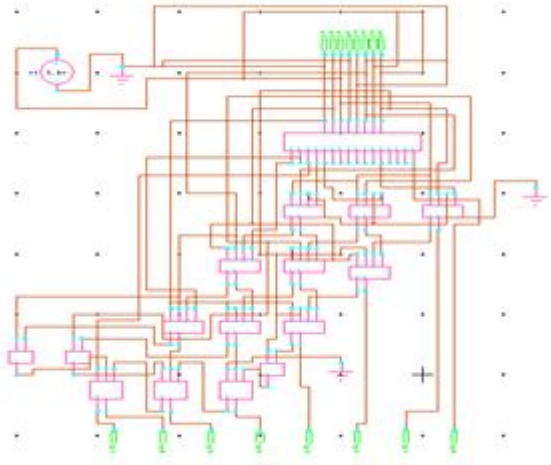

Figure. 7. Design of Column Bypass Multiplier

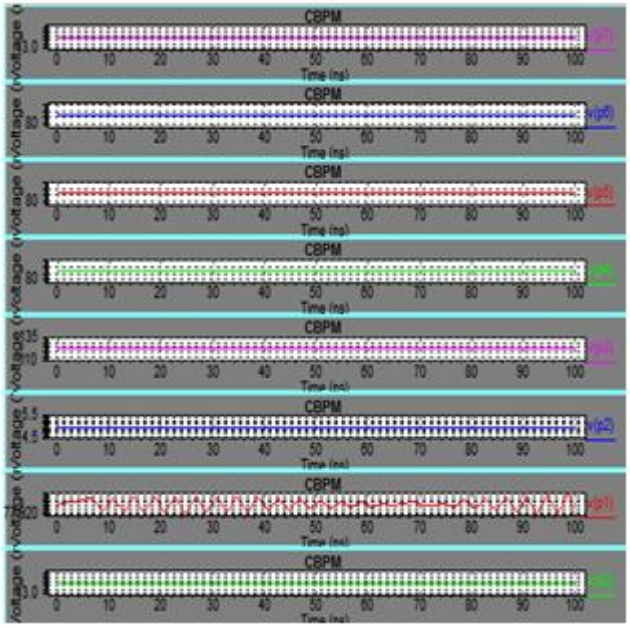

Figure 8:simulation result for column bypass multiplier

Power Results for column bypass multiplier:
Average power consumed -> 1.6461e-05 watts

### *C. Booth multiplier*

Fig. 8 shows the design of booth multiplier using booth recoding unit. The design is created using S-Edit in Tanner. initially, XOR, INV (inverter) and MUX (multiplexer) are created using CMOS logic and by instantiating respective blocks circuit is drawn. In this given multiplier is converted into booth equivalent number by using the booth decoder. The output of the booth decoder is given to the partial product generating unit. Here it will reduce and given to full adder circuit. There output will be evaluated.

In booth multiplier design the design is basically with the increasing the number of zeros. The simulation output of this booth multiplier is shown in the fig. 10 it will get the group of input for x and bit by bit input for the multiplier. The output for the given input is taken through the out.




DOI: 01.IJRTET.9.1.31

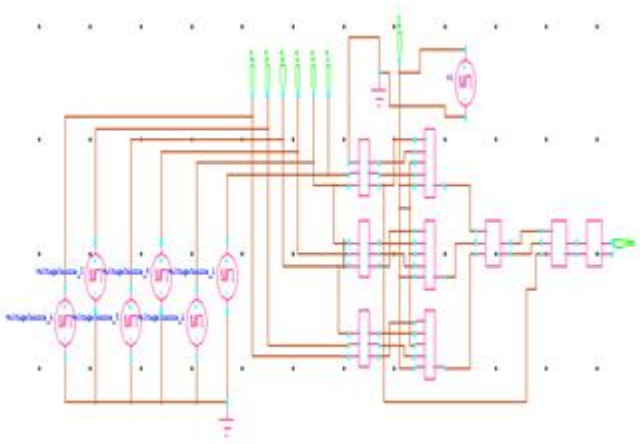

Figure. 9 Design of Booth Multiplier

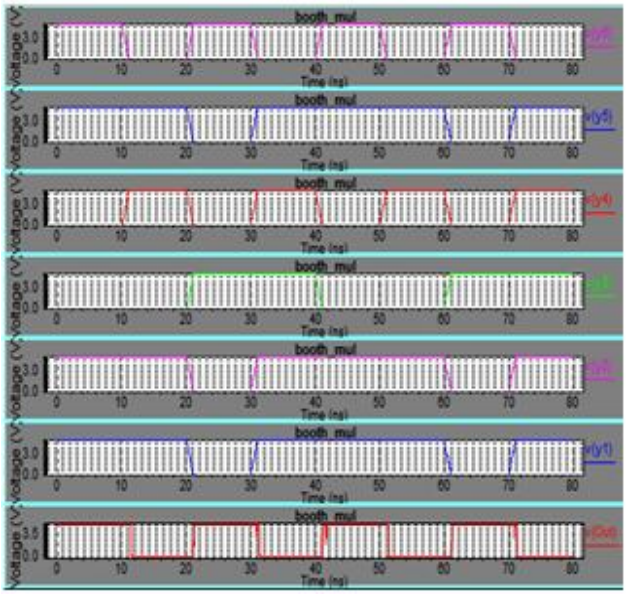

Figure. 10. Simulation Output of Booth Multiplier

Power Results for Booth multiplier:
Average power consumed -> 2.8240e-005. Watts.

*D. Booth Multiplier Using reverse body bias.*

In booth mu;tiplier using reverse body bias technique the average power of the booth multiplier is reduced in which leakage current factor is being reduced.. the circuit required for the design is the same as shown in fig.9 the simulations output of circuit is shown below with the required power results.

TABLE II. Power Analysis

| Input(4-bit Multiplier and multiplicand) | Average Power In uW | | | |
|---|---|---|---|---|
| | Array multiplier | Column bypass multiplier | Booth multiplier | Booth Multiplier with RBB |
| 0011X0010 | 7.14 | 6.42 | 2.85 | 1.14 |
| 0011X0101 | 11.17 | 4.23 | 1.25 | 0.51 |
| 0111X0011 | 11.24 | 4.65 | 1.117 | 0.468 |
| 1110X1101 | 19.48 | 7.69 | 2.73 | 0.83 |

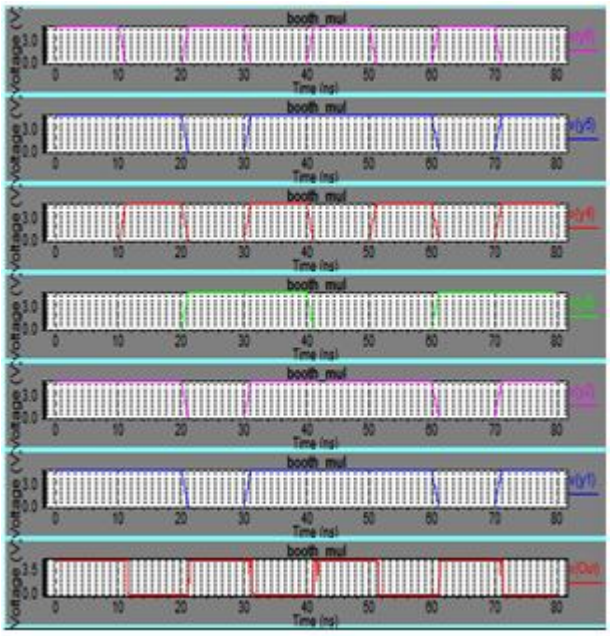

Figure 11 simulation result of booth multiplier using reverse body bias

Power Results for Booth multiplier
Average power consumed: 2.7001e-005 watts

*E .Power Analysis.*

Then the power comparison is for the average power consumed by the each circuit. The comparison is for different input. By varying the multiplier and the multiplicand in the circuit the evaluation is carried out. It is shown below for different input. Table II shows the Average Power Comparison between Different Adders used in Column Bypass Multiplier.

## V. CONCLUSION

In this project, booth multipliers are proposed for reducing the power of the multiplier circuit. The multiplier circuit is designed with conventional full adder. The schematics are drawn and simulated. The power results are thus compared for the different inputs. The result shows that average power consumed by the multiplier. When using booth multiplier technique is less compared to column bypass technique and array multiplier .booth multiplier is also being designed for low power using reverse body bias technique in which the 40% of power is being saved as shown in the table above. Booth multiplier consumes comparatively less power and hence multiplier with booth recoding unit is designed for low power consumption.

## REFERENCES

[1]. M C Wen, S J Wang, and Y N Lin, " Low-Power parallel multiplier with column bypassing ," lEE Electr Lett, vol. 41,pp. 1-2, 2001.

[2] Ohban.J, V.G. Moshnyaga, and K. Inoue, "Multiplier energy reduction through bypassing of partial products," Asia-Pacific Conf .on Circuits and Systems. vol.2, pp. 13-17, 2002.




DOI: 01.IJRTET.9.1.31

[3] Oscal T. -C. Chen, Sandy Wang, and Yi-Wen Wu, "Minimization of Switching Activities of Partial Products for Designing Low-Power Multipliers", IEEE Transactions on VLSI Systems, vol. 11, no. 3, June 2003.

[4] Ming-Chen Wen, Sying-Jyan Wang, and Yen-Nan Lin, .Low Power Parallel Multiplier with Column Bypassing., *Electronics letters*, 10, 12 May 2005 Volume 41, Issue Page(s): 581 -583

[5] Sanjiv Kumar Mangal,Rahul M.Badghare," FPGA Implementation of Low Power Parallel Multiplier",10th International Conference on VLSI Design,2007

[6] Hussain R,Shakkaf A.Y.M, "An efficient modified booth multiplier architecture"ICED 2008

[7] Rao P.V and Cyril Prasanna Raj and S. Ravi, "VLSI Design and Analysis of Multipliers for Low Power", Fifth International Conference on Intelligent Information Hiding and Multimedia Signal Processing, 2009.

[8] Das.D, Rahaman.H "A Novel Signed Array Multiplier"Advances In Computer Engineering 2010 Conference

[9]. Shiann-Rong Kuang and Jiun-Ping Wang "Design of power efficient configurable booth multiplier" IEEE Trans. Circuits Syst. I Regular Papers vol. 57, no.3, pp. 568-580, March 2010.

[10]Vazquez.A,Antelo.E "Improved Design Of High Performance Parallel Decimal Multipliers" IEEE Transactions On Computers,May 2010

[11]Meher.M,Jong Ching Cheun "A High Bit Rate Serial Serial Multiplier With On The Fly Accumulation By Asynchronous Counters"IEEE Transactions On Very Large Scale Integration,Oct 2011.

[13] Tushar V.More, Dr.R.V.Kshirsagar, "Design of Low Power Column Bypass Multiplier using FPGA" IEEE journal of solid-state, circuits, vol 31,pp 1535-1546,July 2011.

[14] Dong-Su Lee, Young-Hyun Jun, and Bai-Sun Kong"Simultaneous Reverse Body and Negative Word-Line Biasing Control Scheme for Leakage Reduction of DRAM" Ieee Journal Of Solid-State Circuits, Vol. 46, No. 10, October 2011

[15]Liyi Xiao,Chang Liu "A Novel Adaptive Body Reverse Body Bias Technique To Minimize Standb Leakage Power And Compensate Process Variations" Cross Starit Quad Regional Science And Wireless Technology Conference,2011

[16]M.N Murthy.S.S Nayak "4 Bit Serial Parallel Multiplier And Bit Level Systolic Architecture For Implementation Of Discrete Orthogonal Transform" Communications In Computer And Information Science Volume 269,2012

[17] N. H. E. Weste, and K.Eshraghain, "PRINCIPLES OF CMOS VLSI Design, A Systems Perspective," Pearson Education, 2010.

[18] M. Morris Mano, "Digital Design" – Third Edition, Prentice Hall of India private limited, 2006

[19]A. P. Chandrakasan and R. W. Brodersen, *Low-Power CMOS Design*. Piscataway, NJ: IEEE Press, 1998.

[20] G. K. Yeap, *Practical Low'-ower Digital VLSI Design*. Norwell, MA: Kluwer, 1998





DOI: 01.IJRTET.9.1.31